UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,315	10/31/2003	Yoshinori Shizuno	OHG 141	9863

23995 7590 09/12/2007

RABIN & Berdo, PC
1101 14TH STREET, NW
SUITE 500
WASHINGTON, DC 20005

EXAMINER	
ARORA, AJAY	

ART UNIT	PAPER NUMBER
2811	

MAIL DATE	DELIVERY MODE
09/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/697,315	SHIZUNO, YOSHINORI	
	Examiner	Art Unit	
	Ajay K. Arora	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8, 10-11, 13-14 & 16-19* is/are pending in the application.

4a) Of the above claim(s) *2--8, 11, 13 & 14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,10 and 16-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

LYNNE GURLEY
SUPERVISORY PATENT EXAMINER
AU 2811, TC 2800

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/10/2007 has been entered. An action on the RCE follows.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 16, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ogawa (US 4,418,284), hereinafter Ogawa in view of Honda (US 2002/0064935), hereinafter Honda.

Regarding claim 1, Ogawa (refer to Figure 3) teaches a semiconductor device comprising:

a semiconductor chip (15);

first pads (6) provided on a main surface of said semiconductor chip;

a light-receiving element (Col. 4, line 33-35) portion (3) provided on said main surface of said semiconductor chip such that a light-receiving surface (3) thereof is exposed;

a light-transmitting portion (7) provided so as to cover the light-receiving surface (3) of said light-receiving element portion for transmitting incoming light to said light-receiving element portion;

an insulating film (13) provides over said main surface of said semiconductor chip;

wiring patterns (wiring part of layer 5 that connects to pads 6) electrically connected to said first pads (6).

However, Figure 3 of Ogawa does not show interconnection details of the first pads (6) to form external terminals, and as such, does not teach interconnection details like "the insulating film surrounding and contacting side surfaces of the first pads", the wiring patterns "extending from said first pad and over said insulating film"; the "post portions", the "sealing layer" and the "external terminals". Honda teaches (refer to Figures 4A-4F) a semiconductor device with a semiconductor chip (11), first pads (comprising 12/21), wiring patterns (comprising 24a) and insulating film (13/20), wherein:

the insulating film (13/20) is surrounding and contacting side surfaces of the first pads (comprising 12/21);

post portions (30) provided on said wiring patterns (comprising 24a), the post portions being electrically connected to the wiring patterns;

a sealing layer (27) provided on said wiring pattern (comprising 24a), on said insulating film (13/20), and on side surfaces of said post portions (30);

the sealing layer (27) surrounding a side surface of said light-transmitting portion (this would follow if the first pads 6 of Figure 3 of Ogawa are modified in view of first pads 12/21 of Figure 4F of Honda and Honda's corresponding interconnection details as explained above); and

external terminals (25) provided on said post portions (30), the external terminals being electrically connected to said first pads via said wiring patterns.

It would have been obvious to one of ordinary skills in the art at the time of the invention to modify Ogawa to incorporate the teachings of Honda as explained above. The ordinary artisan would have been motivated to modify Ogawa for at least the purpose of creating a flip chip mounted package with mounting bumps on the side of the chip with the chip pads, utilizing the post portions to provide the required height of the interconnects.

Regarding claim 16, Ogawa (refer to Figure 3) teaches a semiconductor device comprising:

a semiconductor chip (15) having a first main surface and a second main surface opposed to the first main surface;

a first pad (6) formed on the first main surface of said semiconductor chip;

a light-receiving (Col. 4, line 33-35) element (3) formed on the main surface;

a light-transmitting member (7) provided over said light-receiving element (3), the light transmitting member transmitting incoming light to said light-receiving element;

an insulating film (13) provided over the first main surface, the insulating film surrounding and contacting side surfaces of the first pad;

a wiring pattern (wiring part of layer 5 that connects to pads 6) electrically connected to said first pads (6).

However, Figure 3 of Ogawa does not show interconnection details of the first pads (6) to form external terminals, and as such, does not teach interconnection details like "the insulating film surrounding and contacting side surfaces of the first pads", the wiring patterns "extending from said first pad and over said insulating film"; the "post portions", the "sealing layer" and the "external terminals". Honda teaches (refer to Figures 4A-4F) a semiconductor device with a semiconductor chip (11), first pads (comprising 12/21), wiring patterns (comprising 24a) and insulating film (13/20), wherein:

the insulating film (13/20) is surrounding and contacting side surfaces of the first pads (comprising 12/21);

a post electrode (30) is formed on said wiring pattern (comprising 24a), the post electrode being electrically connected to the wiring pattern;

a sealing layer (27) formed on said wiring pattern (comprising 24a), on said insulating film (13/20), and on side surfaces of said post electrode (30);

the sealing layer (27) surrounding a side surface of said light-transmitting member (this would follow if the first pads 6 of Figure 3 of Ogawa are modified in view of first pads 12/21 of Figure 4F of Honda and Honda's corresponding interconnection details as explained above); and

an external terminal (25) formed on a top surface of said post electrode (30).

It would have been obvious to one of ordinary skills in the art at the time of the invention to modify Ogawa to incorporate the teachings of Honda as explained above. The ordinary artisan would have been motivated to modify Ogawa for at least the purpose of creating a flip chip mounted package with mounting bumps on the side of the chip with the chip pads, utilizing the post electrode to provide the required height of the interconnects.

Regarding claims 18 and 19, if the first pads 6 of Figure 3 of Ogawa are modified in view of first pads 12/21 of Figure 4F of Honda and Honda's corresponding interconnection details as explained above for claim 16, the sealing layer (27 of Figure 4F of Honda) will cover the said light-transmitting member/portion (7 of Figure 3 of Ogawa) and extend above the light-transmitting member/portion so that the post electrode (30 of Figure 4F of Honda) can be formed, as taught by Honda. Therefore, it would be obvious to modify Ogawa in view of Honda (also see rejections of claims 1 and 16), so that the sealing layer directly contacts the side surface of said light-transmitting member/portion. The ordinary artisan would have been motivated to modify

Ogawa for at least the purpose of creating a flip chip mounted package with mounting bumps on the side of the chip with the chip pads and said light-transmitting member/portion, utilizing the post electrode to provide the required height of the interconnects.

Claims 10 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ogawa in view of Honda, and further in view of Lanford (US 5,959,358), hereinafter Lanford.

Regarding claims 10 and 17, Ogawa as modified above teaches substantially the claimed semiconductor device but does not teach that "an oxidation film" is formed on the side surface of said post portions or post electrodes. Lanford teaches copper interconnects or wiring for microelectronic devices, wherein an oxidation film is formed on side surfaces of the interconnects/wiring (Col. 4, lines 1-9). It would have been obvious to one of ordinary skills in the art at the time of the invention to modify Ogawa so that an oxidation film is formed on the side surface of said post portions. The ordinary artisan would have been motivated to modify Ogawa for at least the purpose of creating an inert protective layer that prevents further oxidation of the post portions (Col. 4, lines 1-9).

Response to Arguments

Applicant's arguments of 7/10/2007 with respect to amended claims 1 and 16, and their dependent claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ajay K. Arora whose telephone number is (571) 272-8347. The examiner can normally be reached on Mon through Fri, 8am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on (571) 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LYNNE GURLEY
SUPERVISORY PATENT EXAMINER
AU 2811, TC 2800

AKA

Date: August 20, 2007